REMARKS

Applicants appreciate the Examiner's *extremely* thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Several claims have been amended to better define the claimed invention. Claim 31 has been rewritten in independent form including all limitations of base claim 1, now cancelled. No new matter has been introduced through the foregoing amendments.

The claim objections are believed overcome in view of the above amendments which have been made in view of the suggestions kindly provided by the Examiner in the Office Action.

The *35 U.S.C. 103(a)* rejections over *Nagamura* in view of *Bui* are traversed for at least the reasons presented in the previous Amendment(s) which are incorporated by reference herein for the sake of simplicity.

Notwithstanding the above and solely for the purpose of expediting prosecution, Applicants have further amended the claims, where appropriate, to specifically avoid the Examiner's improperly combined references.

In particular, the *35 U.S.C. 103(a)* rejections of independent claim 1 (now **independent claim 31**) and the respective dependent claims over *Nagamura* and *Bui* are believed overcome, because the applied references singly or in combination do not fairly teach or suggest the feature of claim 31 against which *Nagamura* and *Bui* are not applied.

It should be noted that capacitors 807 and 808 of *Bui* should be used together because the reference does not teach or suggest that the purpose of the circuit can still be achieved if only one of capacitors 807 and 808 is used. Given the resemblance between the *Bui* inverter 802/803/805/806 and each branch 51 and 52 of *Nagamura*, a person of ordinary skill in the art would recognize that if *Bui* was to be combined with *Nagamura* in the manner proposed by the Examiner, a full set of

capacitors 807/808 should be attached to each branch 51 and 52 of *Nagamura*. The resulting circuit would look like the one depicted in attached *Exhibit A*. Clearly, the resulting circuit would fail to teach or suggest the feature of claim 31 that "said at least one voltage responsive switchable capacitor is the only voltage responsive switchable capacitor connected to the control electrode of said one of the first and second transistors" due to the dual capacitor arrangement 807/808 or 807'/808'. Claim 31 is thus patentable over the art.

The *35 U.S.C. 103(a)* rejections of **independent claim 22** and the respective dependent claims over *Nagamura* and *Bui* are believed overcome, because the applied references singly or in combination do not fairly teach or suggest the added feature of claim 22 that "upon a first transition between the first and second intervals: immediately turning off the path of the first transistor." The claim feature finds support in at least FIG. 2 at 84 and 69. The combination of *Nagamura* and *Bui*, if proper, would not allow the path of the transistor to be immediately turned off due to the *Bui* dual capacitor arrangement 807/808 as shown in *Exhibit A*. There would be at least one switched-on capacitor, either 807 or 808, at any time. Such switched-on capacitor would delay the turning-off of the respective transistor. Claim 22 is thus patentable over the art.

The *35 U.S.C. 103(a)* rejections of **independent claim 26** and the respective dependent claims over *Nagamura* and *Bui* are believed overcome for at least the same reason advanced with respect to claim 31.

The *35 U.S.C. 103(a)* rejections of independent claim 1 (now **independent claim 31**) and the respective dependent claims over *Nagamura* and *Love* are believed overcome, because the applied references in combination would fail to teach or suggest "the threshold voltage of said at least one voltage responsive switchable capacitor and the threshold level of said one of the first and second transistors are configured such that, as the voltage changes in a direction to switch said one of the first and second transistors from off to on, said one of the first and second transistors is switched from off to on before said at least one voltage responsive switchable capacitor is switched from the initial finite capacitance value to the substantially open circuit" as previously recited in

claim 1.

Given the resemblance between the *Love* inverter 68/72/76/70 and branch 52 of *Nagamura*, a person of ordinary skill in the art would recognize that if *Love* was to be combined with *Nagamura* in the manner proposed by the Examiner, the *Love* capacitor 80 should be attached to branch 52 of *Nagamura*. Likewise, a PFET capacitor 80' should be attached to branch 51 of *Nagamura*. The resulting circuit would look like the one depicted in attached *Exhibit B*. The person of ordinary skill in the art would recognize that the *Love* capacitor 80 in the combined circuit and the respective transistor 72 of *Nagamura* are of the same type, i.e., NFET. Thus, NFET transistor 72 of *Nagamura* would be *likely* switched from off to on at about the same time as the *Love* NFET capacitor 80 is switched from the initial finite capacitance value (ON) to the substantially open circuit (OFF). This is different from the claimed invention. Claim 31 is thus patentable over the art.

It should be noted that the Examiner's reliance on *Takenaka* and *Yoshizawa* could not cure the deficiency of *Nagamura/Bui* and *Nagamura/Love* combinations. *Takenaka* and *Yoshizawa* teach that the operation of the circuit remain substantially the same if the resistor is move from the source side to the drain side of the transistor. If *Takenaka* and *Yoshizawa* was to be combined with, e.g., *Nagamura* and *Love*, the resulting circuit (refer to *Exhibit B*) would include resistor R2 at the position denoted by Z (and, likewise, resistor R1 at the position denoted by Z'). The capacitor 80 of *Love* remains of the same type as NFET 72 of *Nagamura* and is turned on/off at about the same time as NFET 72, failing to teach or suggest the claimed invention.

The **dependent claims** are considered patentable at least for the reasons advanced with respect to the respective independent claims.

Conclusion

Each of the Examiner's rejections has been traversed. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025 and please credit any excess fees to such deposit account.

Respectfully submitted,

Kenneth KOCH II et al.

Randy A. Noranbrock
Registration No. 42,940
Telephone: (703) 684-1111

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400
Facsimile: 970-898-0640
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RAN/KL/bjs